## 12.3 A 30mW 12b 40MS/s Subranging ADC with a High-Gain Offset-Canceling Positive-Feedback Amplifier in 90nm Digital CMOS

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ADC is a critical block of communication system SoCs. High-resolution ADCs with low power and low supply voltage are required for such applications. Subranging architecture meets these requirements because it does not use the type of closed-loop circuits which restricts low voltage operation. The 12b ADC proposed in this paper is based on a two-step subranging architecture and is composed of a 7b coarse ADC (CADC) and a 6.6b fine ADC (FADC). A high-gain offset-canceling positive-feedback amplifier is used, which allows the ADC to operate with high precision and low power. The total power consumption of the 12b ADC is 30mW (including 10mW for the T/Hs) at a sampling rate of 40MS/s. The energy per conversion-step, defined as Power/($2^{ENOB}\times f_s$), equals 0.69pJ/conversion-step at 40MS/s $f_s$ and 19.9MHz input signal frequency ($f_{in}$), and 0.44pJ/conversion-step at 50MS/s $f_s$ and 1MHz $f_{in}$. Excluding T/Hs, the ADC can operate at 0.7V. The T/Hs (including the switches for the reference ladder) operate at 2.0V.

The block diagram of the proposed ADC is shown in Fig. 12.3.1 The ADC is composed of a 7b CADC with distributed T/Hs, a 6.6b FADC with time-interleaved T/Hs, a reference ladder, a switch matrix, and an encoder. The ADC is comprised of fully differential circuits which have no cascode topologies, since such structures would restrict low-voltage operation. First, the CADC performs 7b quantization of the sampled voltage. Next, the FADC performs quantization of the sampled voltage after the switch matrix connects the FADC to the appropriate subrange of the reference ladder, which is determined by the CADC. The digital encoder combines the CADC and the FADC output data into the final digital output code. Figure 12.3.2 shows the timing diagram.

The CADC consists of 125 comparators preceded by pre-amplifiers, including high-gain offset-canceling positive-feedback amplifiers (PFAs), which greatly reduce the input-referred offsets of the comparators while consuming a low power. The PFA enable the CADC to perform as a high accuracy ADC. In fact, the matching effect of the CADC and FADC in a high-resolution subranging ADC is problematic. The CADC uses two-times interoperation to reduce the number of input capacitors which implement the subtraction of the CADC input signal and the reference voltage. The 7b quantization capability of the CADC reduces the number of the comparators needed for the FADC.

The FADC consists of 97 comparators preceded by pre-amplifiers including the PFAs. The differential amplifiers are auto-zeroed to reduce their offset contribution. The FADC has 2 pairs of time-interleaved sampling capacitors, which consume no additional power [1]. The capacitors of a single pair function simultaneously with each pair used alternately. Also, only two switches are connected to the reference ladder in the comparison phase, which alleviates the influence of the switching noise to the reference ladder. A 5-stage interpolation is implemented for the 2-input-capacitor configuration, leading to a considerable reduction of the input capacitance. The value of the input capacitors is determined by kT/C noise. The number of amplifiers (excluding first source followers) used in each interpolation stage is 3, 5, 17, 49, and 97, respectively.

The ADC power consumption is predominantly determined by the differential amplifiers preceding each comparator, which suppress the random comparator offsets. The input-referred offset voltage of each comparator, $V_{off}$, is given by $V_{off0}/A1$, where $V_{off0}$ is a random comparator offset and A1 is the total gain of the pre-amplifiers including the PFAs. In the conventional design, pre-amplifier power consumption must increase if its gain is increased to reduce the input-referred offset voltage of the comparator. To resolve this problem, a PFA is used. The positive feedback system is implemented by the capacitors shown as "C1" in Fig. 12.3.3. The PFA operates in two non-overlapping phases of $\phi 1$ and $\phi 2$, the reset phase and the amplification phase. During the reset phase, the differential inputs are shorted to the same node, "Va", by the switches designated as "S2," and the gate and drain of the NMOSs "T3" and "T4" are connected by the switches designated as "S3". The offset voltage of differential inputs is stored on C1 and C2. During the amplification phase, the opening of S3 switches change the configurations of T3 and T4 from diode-connected loads to current-source loads. There is no dc path for the positive feedback signals, thereby maintaining the offset canceling function. The PFA has a high gain as compared to the conventional offset-canceling amplifier without increasing power dissipation. Here, the capacitor C2 has three functions. First, it stores the offset of the PFA. Secondly, it transmits the input signal to T3 and T4 without dc, improving the gain of the PFA. Thirdly, it distributes the positive feedback in a manner expressed by the ratio of C1 over C2. The point is that the positive-feedback ratio is decided not by the absolute value of C1 but by the relative values of C1 and C2. This ensures the stability of the PFA independent of the variation of the capacitors. PFA gain increases in proportion to the increase of $(g_{m1}+g_{m2})A$, decreasing the input-referred offset of the following comparator. Here, A is a function of the positive feedback ratio C1/C2 and the comparison time, $g_{m1}$ is the transconductance of T1 and T2, and $g_{m2}$ is the transconductance of T3 and T4. At the same time, the PFA itself decreases its input-referred offset. The gain of the PFA is $g_{m1}/g_{m2}$ in reset phase. The input referred-offset of the PFA is decreased according to the ratio of the reset-phase gain and comparison-phase gain, that is, $(g_{m1}/g_{m2})/((g_{m1}+g_{m2})A) = 1/((g_{m2}+g_{m2}^2/g_{m1})A)$ [2]. Results comparing the conventional design and the PFA-utilizing design (Fig. 12.3.3) are shown in Fig. 12.3.4. As can be seen, the PFA-utilizing design improves gain and input-referred offset drastically. The gain of the PFA-utilizing design is approximately 200 with 10μA current draw and increases according to the comparison-time, while the gain of the conventional design is approximately 15.

The ADC is fabricated in a 90nm digital CMOS process using no analog enhancements. The ADC can operate from a supply as low as 0.7V (excluding the T/Hs). The total power consumption of the ADC is 30mW at a sampling rate of 40MS/s. Figure 12.3.5 shows measured dynamic performance of the ADC and Fig. 12.3.6 shows a performance summary. Figure 12.3.7 shows the die micrograph of the ADC. The active area is $1.98\times2.36mm^2$.

*References:*

[1] Y.T. Wang and B. Razavi, "An 8-bit 150-MHz CMOS A/D Converter," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 308-317, Mar., 2000.

[2] K. Ono et al., "A 6bit 400Msps 70mW ADC Using Interpolated Parallel Scheme," *Symp. VLSI Circuits Dig. of Tech. Papers*, pp. 324-325, June, 2002.

 

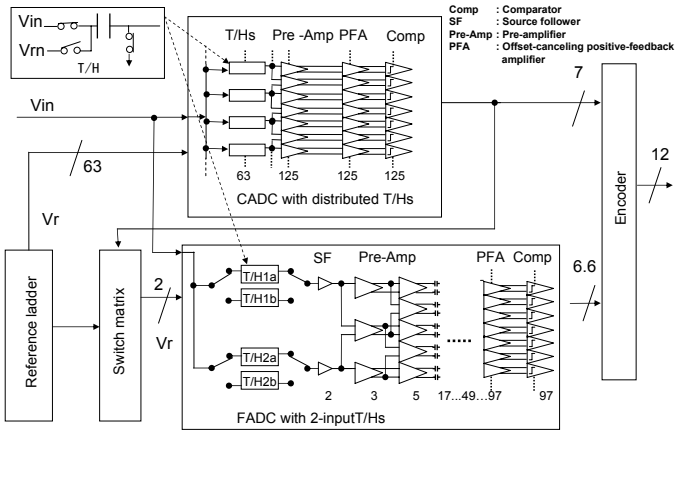


Figure 12.3.1: 12b subranging ADC.

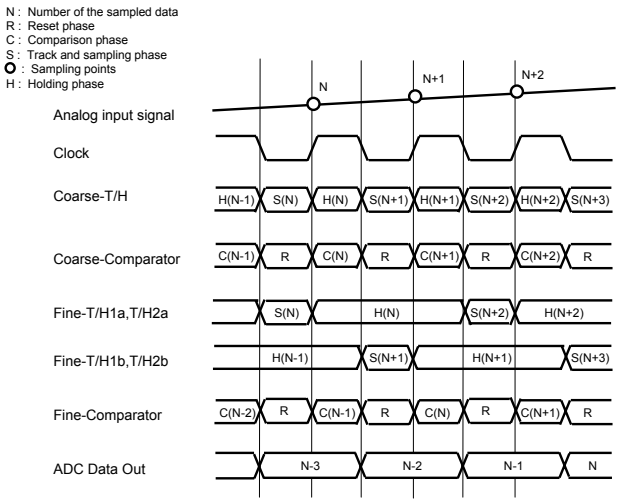


Figure 12.3.2: Timing diagram.



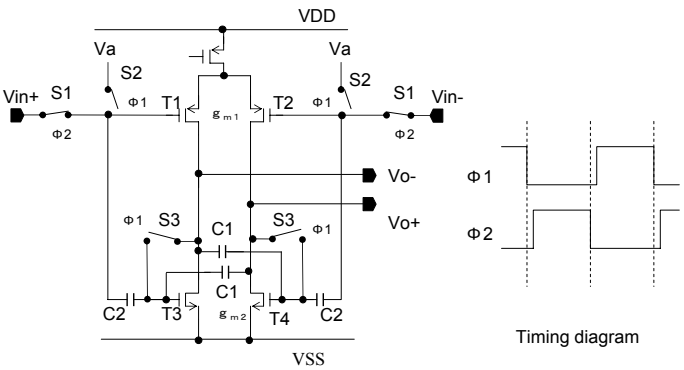


Figure 12.3.3: Offset-canceling positive-feedback amplifier.

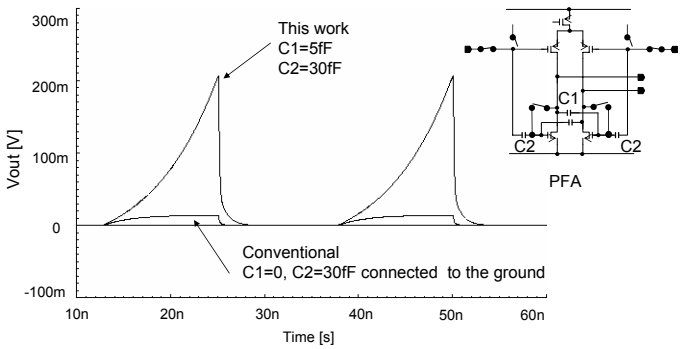


Figure 12.3.4: Differential output signal of the PFA(simulated, input voltage:1mV$_{pp}$, comparison time: 12.5ns, output load capacitance:10fF, and supply voltage:1.0V).

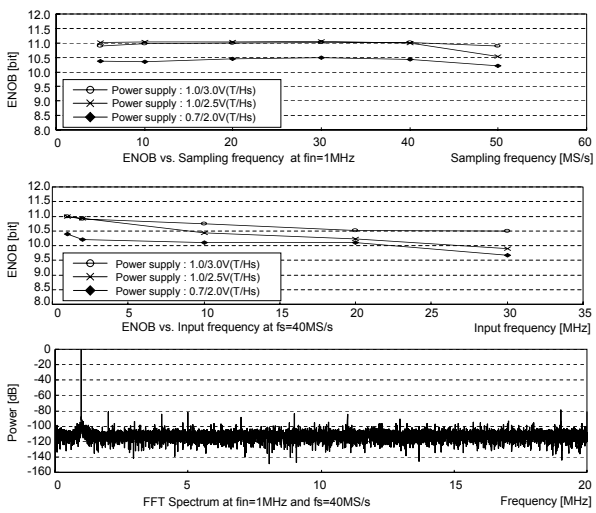


Figure 12.3.5: Measured ENOB and spectrum.

| | |
|---|---|
| Resolution | 12bits |
| Conversion rate | 40MS/s |
| ENOB | 11.0 bits( at $f_{in}$=1MHz, supply voltage 1.0/2.5V)<br>10.1 bits( at $f_{in}$=19.9MHz, supply voltage 0.7/2.0V) |
| SNR | 69.0dB( at fin=1MHz, supply voltage 1.0/2.5V)<br>63.5dB( at $f_{in}$=19.9MHz, Supply voltage 0.7/2.0V) |
| SFDR | 80.0dB( at $f_{in}$=1MHz, Ssupply voltage 1.0/2.5V)<br>72.7dB( at $f_{in}$=19.9MHz, supply voltage 0.7/2.0V) |
| INL | <0.8LSB |
| DNL | <0.35LSB |
| Power consumption | 30mW ( at $f_{in}$=19.9MHz, supply voltage 0.7/2.0V) |
| Active Area | 1.98mm × 2.36mm |
| Process | 90nm Digital CMOS |

Figure 12.3.6: Performance summary.

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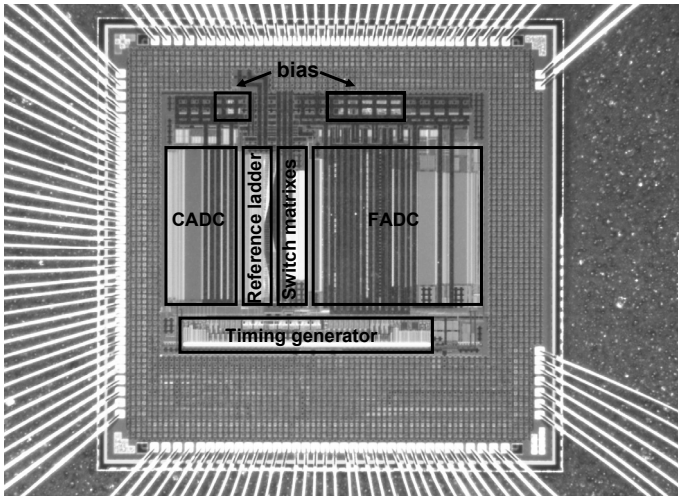


**Figure 12.3.7: ADC die micrograph.**

 